Shield-Based Microwave On-Wafer Device Measurements

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***Abstract*—This paper introduces a shielding technique for use with microwave on-wafer device characterization. This results in a shield-based test fixture, which offers many advantages compared to conventional structures. Among others, the test fixture offers full scalability and very low cost, high measuring accuracy, mitigation of leakage problems associated with lossy substrates, and a large measuring realism. The performance of the shield-based method is demonstrated with measurements on test structures fabricated in low-cost silicon processes.**

***Index Terms*—Analog integrated circuits, calibration, microwave measurements.**

I. Introduction

THE demand for improved on-wafer measuring and characterization techniques is still evident, although much research effort has been dedicated to this particular subject over the last two decades. A commonly used approach to enhance measuring accuracy is to combine two-port calibration performed with an impedance standard substrate (ISS) with an offline correction or deembedding technique. Several deembedding techniques have been proposed over the years, including open pad correction, three-step deembedding [1], [2], and full two-port correction [3].

Recently, a renewed interest in more accurate on-wafer measuring techniques has emerged due to the application of low-cost silicon processes at radio and microwave frequencies. Low substrate resistivity and characteristics of aluminum metallization are of primary concern when conducting microwave device measurements directly on the die or wafer [4], [5]. Furthermore, a characteristic of low-cost processing is that devices usually display low performance per area, e.g., for inductors, capacitors, and MOSFETs. This implies that the used test fixture must fit very large devices, often on the order of 50–400 μm. With large devices and test-fixture gaps, the parasitics of available in-fixture standards become very significant. Consequently, traditional deembedding approaches often lead to large systematic offsets and overestimation [6]–[8]. To accommodate this effect, several new techniques have recently been adopted including on-wafer *in situ* calibration [9] and compensated deembedding [7], [10]. With standard test fixtures, these techniques show promising results when applied to silicon technologies. However, fundamentally speaking, a higher performance gain can be achieved by mitigating imperfections rather than employing post correction.

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In this paper, a shield-based test fixture is proposed that alleviates many of the concerns associated with low-resistivity substrates. The technique was first introduced in [11] and later expanded upon in [12]. In this paper, the features of the shield-based test fixture are detailed and several measuring results are presented, showing good agreement with theoretical and practical predictions. The technique offers: 1) full scalability and very low cost; 2) high measuring accuracy; 3) mitigation of leakage problems associated with lossy substrates; and 4) a large measuring realism.

II. Shield-Based Test Fixture

The basic design goal of the test fixture is to prevent the signal pads from coupling to the substrate. As shall be seen, such measures result in several important advantages. For circuit designs, RF improved pads have previously been suggested that employ variations of shielding techniques [13], [14]. However, the test fixture presented here is optimized for on-wafer measuring performance and further extended to multiport measurements. The isolation of the test-fixture signal pad is achieved by extending a grounded shield below the signal pad, as illustrated in Fig. 1(a). The shield is connected to the ground pads to ensure an accurate on-wafer reference. Although the illustration is made for a ground–signal–ground (GSG) probe, the method is compatible with other types of probes, e.g., ground–signal (GS) and ground–signal–ground–signal–ground (GSGSG), as well.

Note that the shield-based structure is not directly compatible with processes where layout rules dictate that all metal layers be employed in the pad layout. However, since: 1) such rules are associated with large-scale yield and 2) the structure is fundamentally compatible with basic silicon processing, most foundries are willing to fabricate the shield-based fixtures. In fact, RF designers commonly break layout rules in order to achieve adequate microwave pad performance. However, a possible concern is that the absence of metal layers in the center pad may lead to a height difference between ground and signal pads. Common pad design rules for on-wafer probing imply that the height difference between pads should not exceed 0.5 μm [15]. As of this writing, no problems have been observed in practice, although up to five metal layers have been excluded from the signal pad. Further, the required amount of skate is usually on the order of 50–60 μm for aluminum-based pads [5], which, in practice, effectively mitigates the problem. As to facilitate good contact reliability, at least two top metal layers should be incorporated in the signal pad structure. Further, alignment marks should be placed on the die in order to facilitate consistent skate.

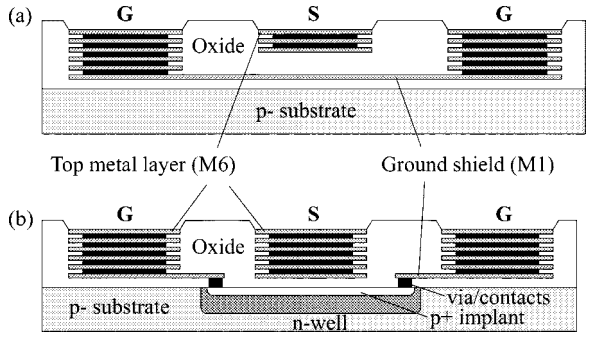

Fig. 1. (a) High-performance and (b) layout rule-compliant shield-based contact pads.

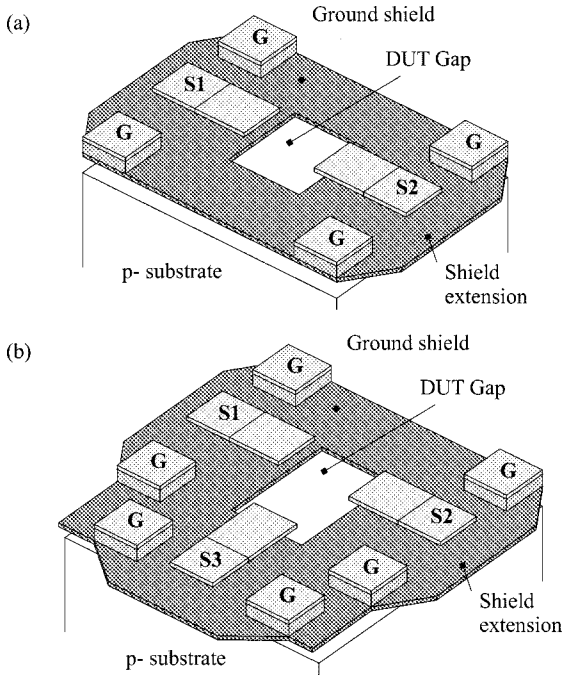

Fig. 2. Shield-based GSG test fixtures minded for: (a) two- and (b) three-port DUT measurements.

For processes where the suggested bending of layout rules cannot be accepted, it is possible to fabricate a compliant structure, as shown in Fig. 1(b). The structure uses a p+ implant under the signal pad, which is connected to the ground pads. With this approach, all metal layers are used in the signal pad layout. An n-well should be used to isolate the grounded area as much as possible from the device-under-test (DUT). Note that the performance of this pad design is much less than for the similar structure in Fig. 1(a). First, the parallel input capacitance is larger and, second, the p+ implant introduces higher resistive loss, which reduces the quality factor of the parallel input characteristic. However, compared to conventional pad structures, a performance gain is still available.

In Fig. 2(a) and (b), the shield-based structure is extended to two- and three-port measurements. An important consideration is to ensure a low-loss common ground among all ports. Besides fulfilling a basic requirement for all multiport measurements, this also facilitates an accurate ground connection for the DUT and the underlying substrate. In order to terminate fringing fields, a shield extension of approximately 2–3 times the pad

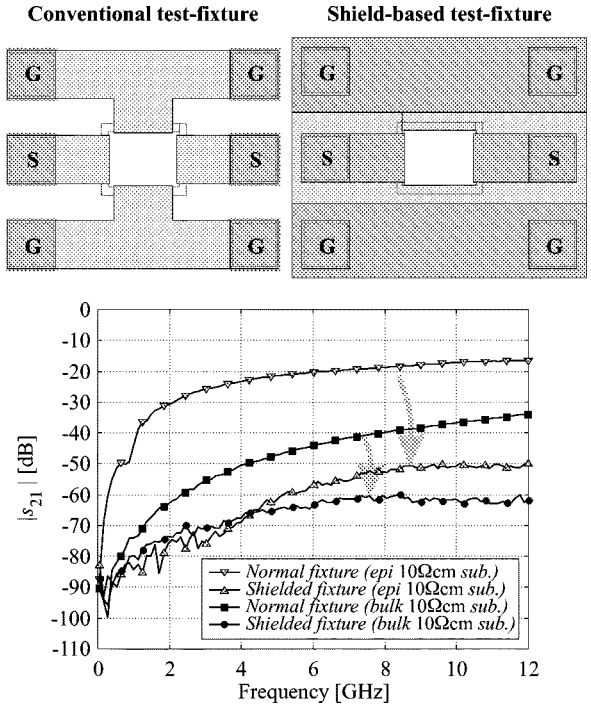

Fig. 3. Reduction in forward coupling by adding ground shield.

height should be used in conjunction with all signal pads. For processes where low-resistivity tungsten is used as the bottom metallization layer, it is advisable to include a second metal layer for lowering the loss of the ground shield. An exception is the area directly below signal leads where a reduced vertical distance would result in an undesired increase in parallel coupling. Further, a smooth transition between pads and input leads is desirable. Input leads should only be drawn in one or two of the top metal layers in order to reduce the susceptibility toward oxide variations.

III. Features of Shield-Based Test Fixture

To demonstrate the capability of the shield-based test fixture, several experiments have been conducted. The most important obstacle to achieving scalable low-cost measurements is the forward coupling of conventional test fixtures. As has been previously demonstrated, this coupling is due to the low resistivity of the silicon substrate and not direct fringing [16], [5]. Hence, the forward coupling is effectively reduced by isolating the signal path from the substrate and making all input ports refer to an accurate common ground. This is effectively demonstrated in Fig. 3, where conventional test fixtures are compared to shield-based test fixtures for two different low-resistivity silicon processes. The bulk process uses dummy patterns and shallow-trench isolation to achieve a fair performance even without the ground shield. However, for many device measurements, a coupling level around -30 dB cannot be neglected and the introduction of the ground shield gives a desirable performance improvement. For the epitaxial process, the coupling is inferior and may even dominate the intrinsic coupling of many devices. Although the improvement of applying shielding is most evident for highly doped substrates, a visible forward coupling reduction is also possible for other common silicon processes.

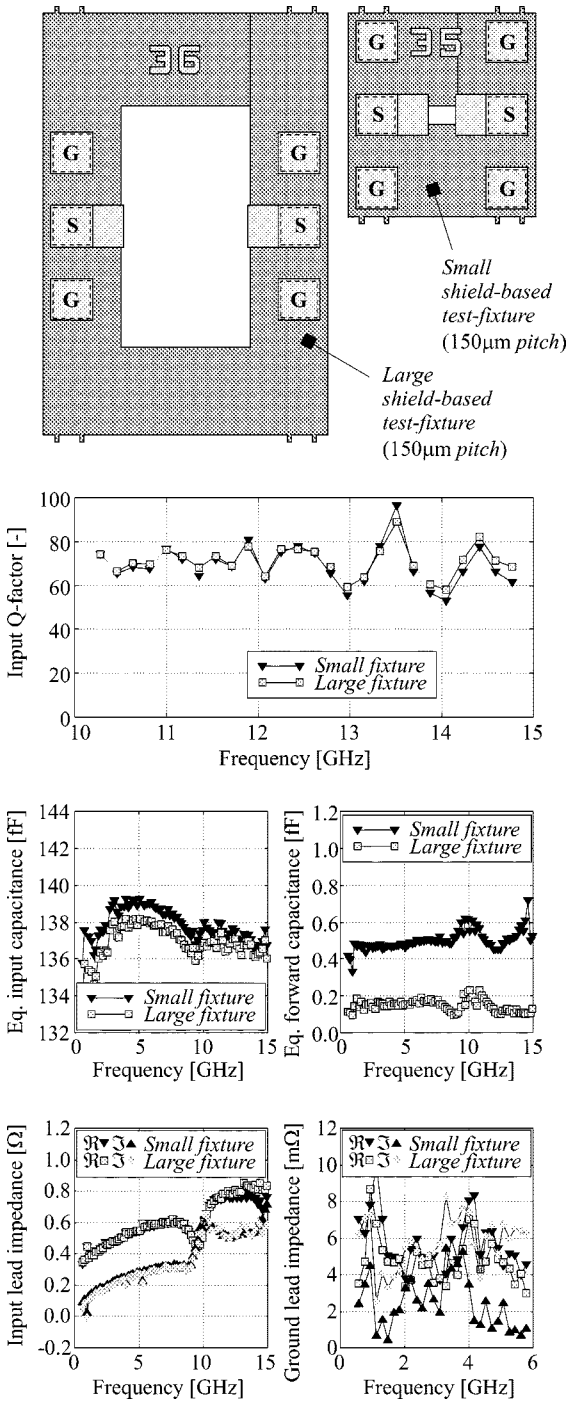

Fig. 4. Test fixture scalability.

The major profit of reducing the forward coupling to very low levels is the achievement of full measuring scalability. By isolating the different input/output ports, all access points to the test fixture can be viewed as independent one-ports. This makes the test fixture scalable in the sense that its parasitics remain constant no matter how large a fixture gap is required for a particular DUT. This aspect is illustrated in Fig. 4 where a very large test fixture is compared to a small test fixture. The sizes shown are typical for inductor and common-source MOSFET measurements, respectively. Series and parallel effects of both test fixtures have been measured and averaged over ten samples. The extraction has been performed by fabricating both full short and full open standards [1]. Note from the comparison that the two test fixtures display similar parasitics. The differences seen in the input capacitance and quality factor is well within process tolerances. The slightly higher absolute capacitance value (although below 1%) may be explained by the layout of the smaller test fixture where more ground shield is placed in the vicinity of the lead ends. Note that the quality factor of the input capacitance is very high, above 60 and around 15 GHz. As the probes and leads are much closer, observe that the smaller test fixture has a slightly higher forward coupling. Still, the equivalent capacitance is well below 1 fF and, hence, negligible for most practical considerations. Note further, that the wide ground shield also gives a very small parasitic series impedance between ground pads and the edge of the fixture gap, which is known as the ground lead or dangling leg impedance [17]. Values below 10 mΩ can usually be neglected even for sensitive common-source MOSFET measurements. Compared to conventional test fixtures, the shield-based fixture gives a reduction of ground lead parasitics on the order of 10–100 times. The ultimate consequence of these results is that only one set of deembedding standards (test structures) is required in order to deembed devices of all physical sizes. This gives a significant cost reduction in comparison to many well-known on-wafer measuring techniques.

Since the substrate interaction has been effectively mitigated, the forward coupling mechanisms are reduced to direct fringing and substrate coupling near the edges of the test-fixture gap. Although small in an absolute sense, it appears that the edge-based substrate-carried coupling dominates direct fringing in practice. However, it has been verified that the forward coupling remains typically below -50 dB for fixture gaps down to 10–15 μm. For device measurements where a forward coupling level of -50 dB at frequencies on the order of 18 GHz is not negligible, its value must be considered and proper correction applied [16].

From the conducted experiments, it is evident that the shield-based test fixture effectively mitigates many of the concerns of conventional test fixtures. To illustrate its simplicity in terms of modeling, a shield-based test fixture has been fabricated in a three-metal-layer 10-Ωcm epitaxial process. The design details are shown in Fig. 5(a). Note that small holes have been chopped out of the ground shield in order to meet a maximum linewidth restriction of the process. The equivalent lumped-element model for the structure has been extracted from measurements and is shown in Fig. 5(b). The model is valid only for 70-μm skate where the frequency dependency of the contact resistance is small compared to the input lead impedance. For smaller amounts of skate, it is often recommendable to include a frequency dependency in the resistance term. At frequencies beyond 10–15 GHz, skin effects make such precautions necessary. Since the process only offers three metal layers, the equivalent input capacitance is quite high, on the order of 0.3 pF. As seen in Fig. 5(c) and (d), there is a high agreement between the model and actual measurements. Hence, the test fixture may be represented by a very simple model.

Compared to conventional test fixtures where the input admittance is influenced mainly by oxide in conjunction with substrate, the input characteristic of the shield-based test fixture

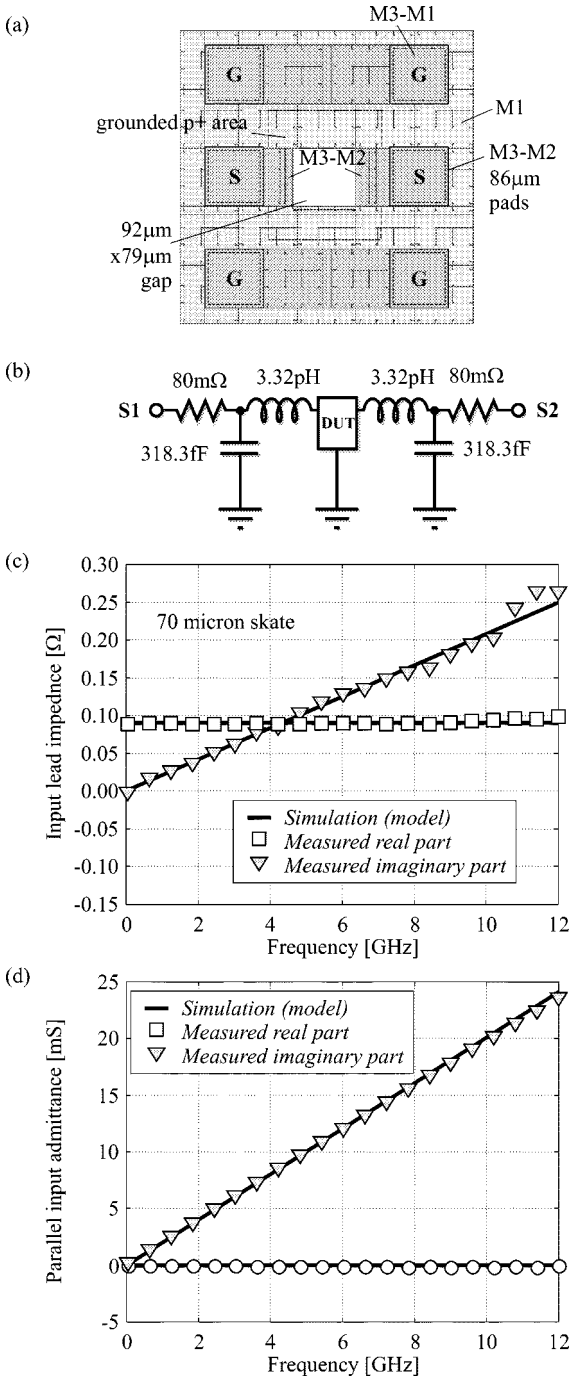

Fig. 5. (a) Fabricated test structure. (b) Equivalent model. (c)–(d) Comparison of model with simulations.

is influenced only by the oxide layer. As illustrated in Fig. 6, this often leads to an increase in the relative tolerances of the input characteristic. An increase by a factor of 1.5–2 is not uncommon. If the test fixture displays a very large input capacitance, this may significantly degrade the dynamic range of the device measurement. However, for modern processes where 5–6 metal layers are typically available, the absolute capacitance level may be reduced significantly compared to a conventional test fixture so that the total absolute tolerances in fact become lower. Still, it is generally advisable to employ statistical techniques when measuring devices fabricated in low-accuracy processes.

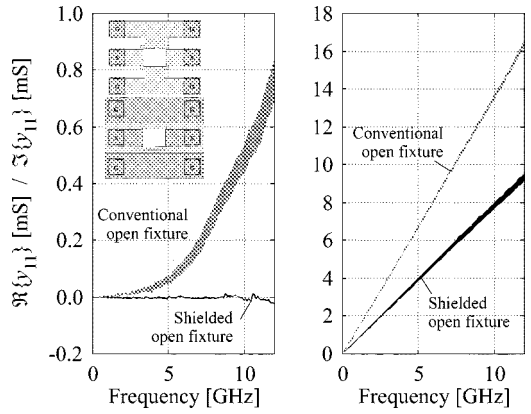

Fig. 6. Comparison of conventional and shield-based test fixture in terms of tolerances.

Due to the input characteristics of the shield-based test fixture, there are several advantages in terms of device measurements. By employing shielding, the resistive effects of the test fixture are heavily reduced. As explained from noise deembedding theory [18], this reduces the impact that the test fixture has on the measured noise figure. The original attempts of using pad shielding in circuit applications [13], [14] have, in fact, been driven by noise considerations. Further, the use of shielding mitigates the potential leakage effects, which can be observed for low-resistivity substrates [5]. With the shield-based structure, the substrate can, therefore, be grounded in a fashion that is most realistic for the DUT. Radio-frequency integrated-circuit (RFIC) designers often surround the devices with substrate taps and a bottom metal layer ground shield in the actual circuit layout. Since this is very similar to the mounting of the device in the shield-based test fixture, a high degree of measuring realism is facilitated. Further, this can be important for processes that employ dummy patterns that apparently significantly affect the performance of RF devices. Finally, since it is possible to reduce the fixture parasitics by using the shield-based method, a lower overall tolerance level and, hence, a higher accuracy for the measurement, are achieved.

IV. Correction Methods

The design of the shield-based test fixture does not limit the measuring method to a subset of correction techniques. For instance, the fixture can be used for implementation of on-wafer thru-reflect line (TRL) microstrip calibration standards. Since the forward coupling is effectively reduced, the test fixture, in fact, fulfills a basic requirement for most two-port calibration methods. However, for practical reasons, full two-port calibration has a limited scope of applicability. Due to on-wafer tolerances, the performance per used area is typically lower than what can be achieved with fixture-optimized deembedding methods. Further, two-port calibration techniques are not easily applied to multiport measurements, which are used with many devices; e.g., for the characterization of MOSFETs. For these purposes, ISS calibration associated with specific deembedding is usually preferable. In the particular case of deembedding, the shield-based test fixture offers some very

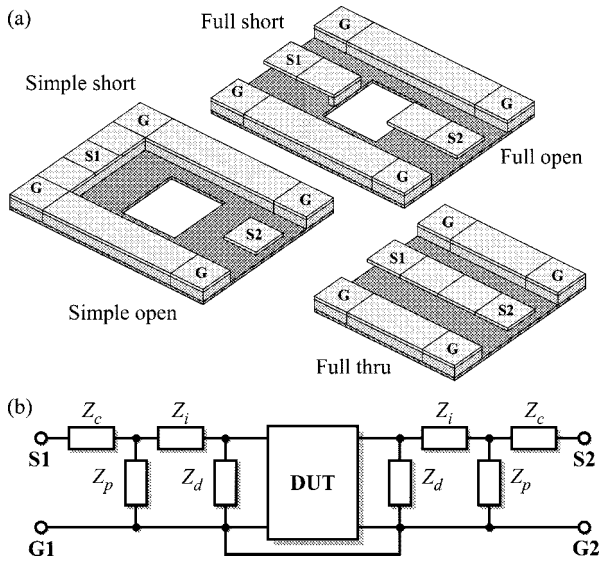

Fig. 7. (a) Accurate in-fixture standards suggested for two-port deembedding. (b) Equivalent model topology for the shield-based test fixture.

important improvements over conventional fixtures, some of which include the following.

- With the effective reduction of forward coupling and ground lead impedance, the accuracy/area ratio of using deembedding is significantly improved.
- Since the shield is available everywhere in the fixture layout, it is possible to implement a highly accurate short standard using a thin stacked array of via. This is illustrated in Fig. 7(a).
- Since ground leads display low parasitic impedance, a very accurate thru standard can be fabricated by directly connecting the two leads of the original test fixture. This is illustrated in Fig. 7(a).
- With a negligible forward coupling, each test-fixture input/output port can be viewed separately. Hence, multiport deembedding with a simple set of in-fixture standards is facilitated.

A higher accuracy of the in-fixture standards directly translates into higher measuring accuracy. Although many different in-fixture standards can be suggested, the set shown in Fig. 7(a) appears to give good practical results. A simple short/open standard is used to isolate the pad effects [7]. This is a convenient way to: 1) verify the ISS calibration and 2) ensure symmetry of extracted parasitics in the case that two probes are worn differently (e.g., unequal contact impedance per skate). The full open/short and thru standards can be used to extract and verify remaining effects shown in the impedance-based model in Fig. 7(b). This equivalent model topology appears to cover most practical device measurements.

Verification of on-wafer measurements using low-accuracy processes is a difficult, but nevertheless important, topic. One suggested method is to employ matching of closely spaced devices in conjunction with general scaling theory [16], [5]. Such a scaling test with highly consistent MOSFET devices (based on a 20-μm unit transistor) has been conducted, and the results are shown in Fig. 8. Note that the devices scale accurately down to very narrow devices in both parallel and forward directions.

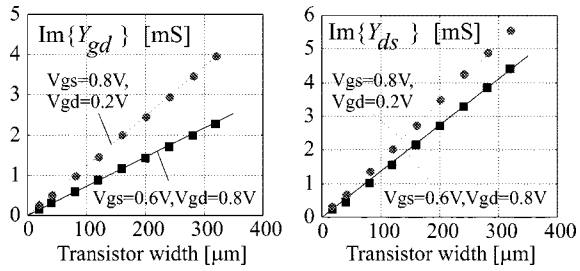

Fig. 8. Measured scalability of varying-width 0.25-μm-long MOSFETs mounted in shield-based test fixtures.

This indicates an accurate deembedding of all parallel parasitics. Hence, the shield-based test fixture effectively settles the dispute of forward coupling compensation [17], [16].

V. Conclusions

A shield-based test fixture has been presented in this paper, which effectively mitigates the substrate-carried coupling and ground lead parasitics. The fixture displays a purely capacitive input characteristic, which facilitates simplified deembedding and noise measurements. Due to an effective reduction of forward coupling, the test fixture enables scalable measurements where the actual performance of multiple-sized devices can be extracted from a single set of on-wafer test structures. This gives a significant cost reduction compared to conventional techniques. The shield-based test fixture supports accurate two-port calibration methods, as well as deembedding techniques. Since in-fixture standards can be fabricated with negligible parasitics, the shield-based method offers a very high accuracy at low complexity. Since the substrate can be configured in a way similar to the real-life application of the device, the test fixture offers a high degree of measuring realism. The performance and scalability of the method have been demonstrated with measurements on test structures fabricated in low-cost silicon processes.

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